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A HIGH-PEROMANCE AND LOW-POWER PIPELINE VEDIC MULTIPLIER USING ADIABATIC LOGI

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Abstract

In this paper, we portray a vitality proficient Vedic multiplier structure utilizing Energy Efficient Adiabatic Logic (EEAL). The power utilization of the proposed multiplier is essentially low on the grounds that the vitality exchanged to the heap capacitance is generally recuperated. The proposed 8x8 CMOS and adiabatic multiplier structure have been planned in a TSMC 0. 18 µm CMOS process innovation and checked by Cadence Design Suite. Both simulation and estimation results confirm the usefulness of such rationale, making it reasonable for implementing energy-mindful and execution - effective very-substantial scaling proportion (VLSI) hardware. The conventional and pipeline Adiabatic Vedic multiplier were discussed in this article.

Keywords: Multiply – Adiabatic logic, Pipeline, multiplier, Vedic Multiplication, CMOS, single phase, low-power.

I. INTRODUCTION

A plenty of augmentation calculation has been proposed as of late in writing [1]-[8]. In this paper we exhibit a methodical outline technique for quick and ar ea effective burrow it multiplier in view of Vedic tangle schematics [3],[4],[9]-[12]. The Multiplier Architecture depends on the Urdhva-Tiryakbhyam [9], sutra or "Vertical and Crosswise" calculation of antiquated Indian Vedic Mathematics. Conventional, as w ell as, adiabatic 8×8 Vedic multiplier structure have been implemented in TSMC 0.18µm CMOS innovation, utilizing CADENCE Design suite.

Adiabatic switching [13]-[15] has as of late happened to a specific intrigue, and is being actualized in numerous frameworks. The approach depends on a moderate charging of the capacitive hubs by time-fluctuating timed air conditioning power and a fractional recuperation of the vitality utilized by gradually diminishing the supply without giving up clamor insusceptibility and driving capacity. In this paper, Energy effective adiabatic rationale (EEAL) in view of DCVS rationale [16], has been presented as an adiabatic rationale style. EEA L requires just a single sinusoidal power clock supply, has straightforward usage, and is intended for rapid and low-vitality VLSI outline. In EEAL, rapid operation and in addition low vitality utilizations are guaranteed by utilizing a parallel resistive way between the yield hubs and clock supply. EEAL rationale highlights straightforwardness and static rationale took after trademark s, which significantly diminishes transistor overheads and the circuit unpredictability.

The rest of the paper is organized as follows. Section II descri bes the operation of EEAL inverter and addresses the issue of power dissipation of this proposed logic. Section III shows the general implementation of N×N Vedic multiplier based on

Urdhva-Tiryakbhyam sutra or "Vertical and Cross wise" algorith m. Implemen tation of co nventional and adiaba tic 8×8 multiplier, experimental results and comparison of performance of our energy recovery logic with other imperative logic styles are also detailed in section IV. Finally, conclusions are given in section V.

II. ENERGY EFFICIENT ADIABATIC LOGIC (EEAL)

Adiabatic circuits are low power circuits which utilize "reversible rationale" to moderate energy. Not at all like conventional CMOS circuits, which disseminate vitality amid exchanging, adiabatic circuits decrease scattering by following two key principles:

1. Never turn on a transistor when there is a voltage potential between the source and deplete.
2. Never kill a transistor when current is coursing through it.

While this is a zone of dynamic research, ebb and flow systems depend intensely on transmission doors and trapezoidal timekeepers to accomplish these objectives. There are a few important principles that are shared by these low-control adiabatic frameworks. These incorporate just turning switches on when there is no potential contrast crosswise over them, just turning turns off when no current is moving through them, and utilizing a power supply that is equipped for recouping or reusing vitality as electric charge. To accomplish this, as a rule, the power supplies of adiabatic rationale circuits have utilized steady current charging (or an estimate thereto), as opposed to more customary non-adiabatic frameworks that have by and large utilized consistent voltage charging from a settled voltage control supply. The power supplies of adiabatic rationale circuits have additionally utilized circuit components equipped for putting away vitality.

This is frequently done utilizing inductors, which store the vitality by changing over it to attractive transition. There are various equivalent words that have been utilized by different creators to allude to adiabatic rationale sort frameworks, these include: "Charge recuperation rationale", "Charge reusing rationale", "Clock-fueled rationale", "Vitality recuperation rationale" and "Vitality reusing rationale". On account of the reversibility necessities for a framework to be completely adiabatic, a large portion of these equivalent words really allude to, and can be utilized between variably, to depict semi adiabatic frameworks. These terms are compact and obvious, so the main term that warrants facilitate clarification is "Clock-Powered Logic". This has been utilized in light of the fact that numerous adiabatic circuits utilize a joined power supply and clock, or a "power-clock". This a variable, as a rule multi-stage, control supply which controls the operation of the rationale by providing vitality to it, and along these lines recuperating vitality from it.

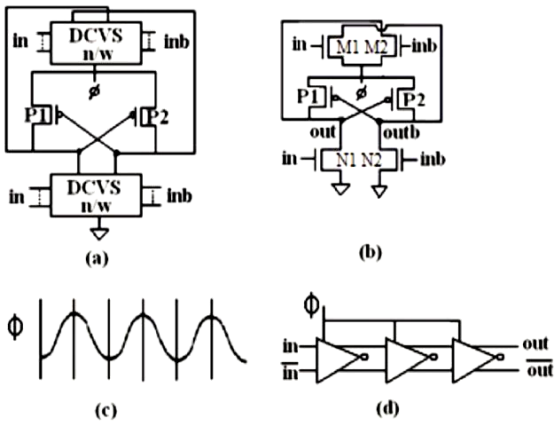

Fig1. EEAL Logic (a) Block Diagram (b) Inverter/Buffer circuit

EEAL requires just a single sinusoidal power clock supply, has straightforward execution, and performs superior to the beforehand proposed adiabatic rationale families [13]-[15] as far as vitality utilization. As single-clock circuit requires straightforward clock plot [16], this rationale style can appreciate minimal control overheads. figure 1

(b) and (c) shows the EEAL cradle/Inverter circuit and supply clock (Φ) separately.

The operation of EEAL inverter/support can be abridged utilizing figure 1 (b). Expecting the reciprocal yield hubs ("out" and "outb") are at first low and supply clock (Φ) increase from logic 0 (" 0") to logic1 ("VDD") state. Presently if "in" = "0" and "inb"= "1"; N1, M1 will be switched OFF and M2, N2 and P1 will be Switched ON. The "out" hub is then charged by following the supply clock (Φ) firmly through the parallel combination of PMOS (P1) and NMOS (M2), while "outb" hub is kept at ground potential, as N2 seems to be "On". At the point when the supply clock swings from "VDD" to ground, "out" hub is released through the same charging path and un-driven "outb " is kept at same ground potential. Resultantly full swing can be acquired in "out" hub and ground potential at "outb" hub. Yield voltage swing for an adiabatic inverter at 100 MHz frequencies with 20 fF capacitive load is shown in fig. 2.

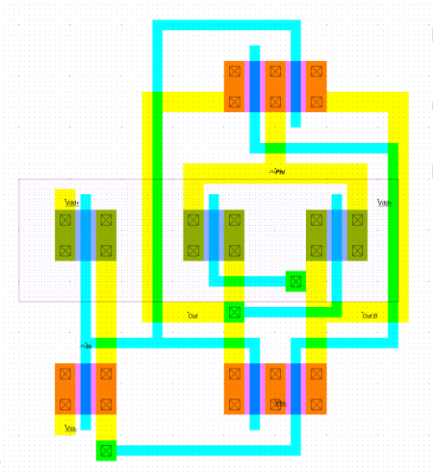

Fig2.CMOS Layout of EEAL Inverter at 180nm

The vitality favorable position of EEAL circuit can be promptly comprehended by expecting an incline sort voltage source which increase in the vicinity of "0" and "V_{DD}" and delivers the stored charge C_LV_{DD} over a day and age T. The dispersal through the channel protection R is,

$$E_{diss}= \{(C_LV_{DD})/T\}^2RT = \{(RC_L)/T\}C_L(V_{DD})^2$$

So also, vitality utilization amid charging or releasing procedure of the EEAL inverter/cradle can be described as,

$$E = \{ (R_PC_L)/T\} C_L V_{DD})^2 + ½ C_L (¨ΔV)^2 \quad (2)$$

Subsequently R_P is the turn-on protection of the parallel way, C_L is the yield stack capacitances, T is the charging time and ΔV is the voltage drop over the resistive way. In spite of the fact that ΔV relies upon time, yet because of little extent (~ few millivolt) the para meter is dealt with as steady. In condition (2), $(½CL(¨ΔV)^2)$ measures the edge misfortune which is insignificantly little in fact. In EEAL as charging and releasing procedures expend practically comparative measure of vitality, add up to vitality dissemination for a complete cycle can be communicated as,

$$E_{load} = 2\{(RC_L)/T\} C_L(V_{DD})^2 + C_L (¨ΔV)^2 \quad (3)$$

Contrasted with regular CMOS rationale, which expends $C_LV_{DD}^2$ vitality in a full cycle (CL is stack capacitances), adiabatic pick up (G) of EEAL progresses toward becoming,

Adiabatic Gain (G) in (%)

$$= \frac{\text{Energy comsumption by EEAL per cycle}}{\text{Energy Consumption by conventional CMOS per cycle}} x100$$

$$= [\{2R_PC_L/T\} + \{(\Delta V)/V_{DD}\}^2] \times 100$$

$$= 2\{R_PC_L/T\}\times 100 \ \ (\text{as } \Delta V<<V_{DD}, \{(\Delta V)/V_{DD}\}^2<<1) \quad (4)$$

So, the adiabatic pick up can be enhanced significantly by dragging out T. Subsequently, the turn-on protection (RP) of the charging or releasing way comprises of parallel mix of PMOS/NMOS transistors and can be communicated as,

$$R=\{\mu_n C_{ox}(W/L)_n(½V_{DD}-V_{tn})+\mu_pC_{ox}(W/L)_p(½V_{DD} -ŇV_{tp}Ň)\}^{-1}=\{\mu_n C_{ox}(W/L)_n(V_{DD} -2V_T)\}^{-1} \quad (5)$$

where (W/L)n ((W/L)p), μ_n (μ_p), V_{tn} ($ŇV_{tp}Ň$) are the aspect ratio, mobility and the threshold voltages of NMOS (PMOS) respectively; all the other terms have the usual meaning. For 0.18µm CMOS

(1)

process, considering V_{DD}=1.8V and $(W/L)_p=2(W/L)_n$, the above expression gives R= 1.02KΩ.

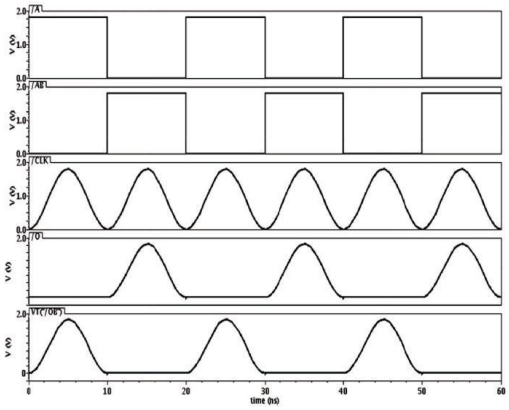

Fig 3. Output waveform rms of EEAL inverter at 100 MHz frequencies with a load of 10fF

III. IMPLEMENTATION OF NXN MULTIPLIERS STRUCTURE

3.1 Urdhva Tiryakbhvam Sutra:

The proposed multiplier depends on a calculation Urdhva Tiryak bhyam (Vertical &Crosswise) [9], a general multiplication formula of old Vedic mathematics. The parallelism in generation of partial products and their summation is acquired utilizing Urdhva Tiryakbhyam clarified later. Since the fractional items and their entireties are figured in parallel, the multiplier is autonomous of the clock recurrence of the processor. It is exhibited that this design is very proficient as far as silicon range/speed. The 2×2 or 4 ×4 duplication using ordinary numerical strategies (progressive augmentations when utilized on PCs) needs no clarification. Henceforth, the Vedic strategy for 4×4 duplication is represented in the case underneath, appeared in Figure 3. Thus, digits of multiplier and multiplicands are put in two successive sides (along push a d section) of a square. If there should arise an occurrence of N×N duplication (subsequently N=4), entire square will be partitioned into N2 (=16) no. of squares, which will be apportioned again by across line, as appeared in Figure 3. Every digit of the multiplier is then freely duplicated with each digit of the multiplicand and the two-digit item is composed in the little square box. Every one of the digits lying on a transversely dabbed line are added to the past convey. The minimum noteworthy digit of the got number acts a s the outcome bits and the rest as the convey for the subsequent stage. In this above illustration beginning is taken as "logic 0". So the adiabatic pick up can be enhanced significantly by dragging out T. Subsequently, the turn-on protection (RP) of the charging or releasing way comprises of parallel mix of PMOS/NMOS transistors and can be communicated as,

$$R=\{\mu_n C_{ox}(W/L)_n(½V_{DD}-V_{tn})+\mu_p C_{ox}(W/L)_p(½V_{DD}-\check{N}V_{tp}\check{N})\}^{-}$$

$$^{1}=\{\mu_n C_{ox}(W/L)_n(V_{DD}-2V_T)\}^{-1} \quad (5)$$

where (W/L)n ((W/L)p), μ_n (μ_p), V_{tn} ($\check{N}V_{tp}\check{N}$) are the aspect ratio, mobility and the threshold voltages of NMOS (PMOS) respectively; all the other terms have the usual meaning. For 0.18µm CMOS process, considering V_{DD}=1.8V and $(W/L)_p=2(W/L)_n$, the above expression gives R= 1.02KΩ.

3.2 Implementation Of General Vedic Multiplier Structure:

In this section we first discuss the association of 2×2 multiplier square, w hich will be additionally utilized to arrange 4×4 and 8×8 multiplier structures. In 2×2 multiplication, considering two inputs (X and Y) having two digits each (X→X1X0 and Y→Y1Y0), we get four yields (S→S4S3S2S1) as a result, by doing vertical and cross-augmentation and expansion.

The steps are:

i) S1 is the aftereffect of Vertical duplication amongst X0 and Y0.

ii) S2 is the expansion of crosswire bit multiplication of (X1 and Y0) and (X0 and Y1).

iii) S3 is the vertical item of X1 and Y1, if no carry is quality appraised from the past advances, generally carry bit willbe added with the vertical item to produce S3 as an aggregate.

iv) S4 is the convey generated during expansion of S3.

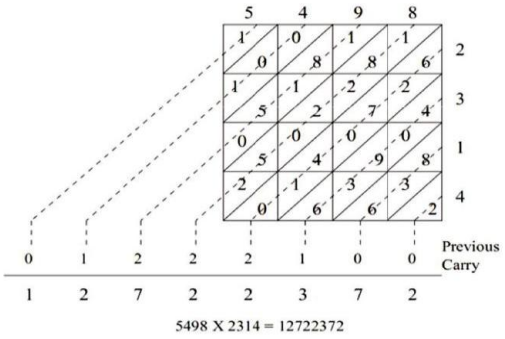

Fig. 4. Multiplication using Urdhva Tiryakhbhyam Sutra

By utilizing this 2×2 multiplier piece 4×4, 8×8, 16×16 and so forth multiplier square can be actualized. For N×N augmentation, appeared in figure 4, N-bit multiplier and multiplicand first will be partitioned into two equal parts, consisting of N/2 no. of bits in each split. Accepting N-bit duplication amongst X and Y, we get XL= {X1 X2 X3…. XN/2} and XH= {X (N/2+1) X (N/2+2) X (N/2+3)… .XN}as two parts of X. For Y, its two parts will be YL={Y1 Y2 Y3… Y N/2} and YH={ Y(N/2+1) Y(N/2+2) Y(N/2+3) … .YN}. Along these lines, X and Y can be spoken to a s XH XL and Y HYL . Presently the means a re given roar,

1)First vertical multiplication between XL (N/2 bits) and YL(N/2 bits) will create tot al N no. of bits. Out of these first N/2 bits {SLL(1) SLL(2) … ..SLL(N/2)} are taken as first N/2 yields {S1 S2 … .SN}. Keep going N/2 bits will be utilized for N-bit in subsequent stages.

2)In subsequent stages cross-increases have done between (X ,Y L) and (XL, YH)to produce two sets of N no. of bits, { SHL(1) SHL(2) SHL(3)… ..SHL(N)} and {SLH(1) SLH(2) SLH(3) … . S LH(N)} respectively. These two sets of N no. of bits are meant create another N no. bits, S11 to S1N and C1 as carry.

3) Vertical increase between XH (N/2 bits) and YH (N/2 bits) likewise creates N no. of b its, {S_{HH} (1) S_{HH} (2) … ..S_{HH}(N)}. Out of these N bits, first N/2 bits, S_{HH} (1) to S_{HH}(N/2) are cascaded with the last N/2 bits, {S_{LL}(N/2+1) S_{LL} (N/2+) …. SLL(N)}, of vertical increase amongst XL and YL. These add up to no. bits will be included with the yield of first N bit viper, S11 to S1N, to master duce add up to N no. of bits (from S(N/2+1) to S (3N/2)) of N×N multiplier. This second N bit expansion likewise produces a convey, C2.

4) C_1 and C_2 are sent to the half adder to generate sum and carry bits. (N/2-2) no. of zero s will be inserted before carry and sum to produce a set of N /2 bits, as shown in figure 4. These N/2 bits will be added up by a N/2-bit adder with the last N/2 bits of vertical multiplication between X_H and Y_H, which are {$S_{HH\ (N/2+1)}$ $S_{HH(N/2+2)}$ …. $SHH_{(N)}$}. The outputs of these N/2 bits addition will produce the last N/2 bits (from $S_{(3N/2+1)}$ to $S_{(2N)}$) of N×N multiplier.

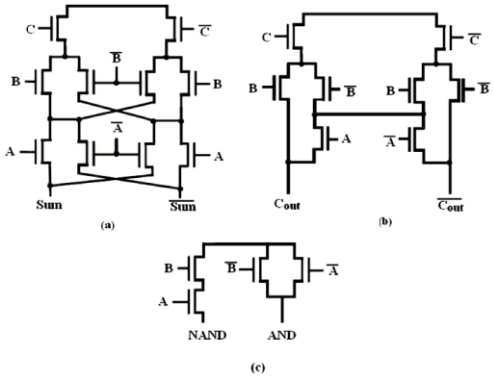

Fig. 5 DCVS network (a) Sum block (b) Carry block (c) AND NAND block

So, in a N×N multiplication, we need four N/2×N/2 multipliers, two N bit adders, a ha lf adder and a N/2-bit adder.

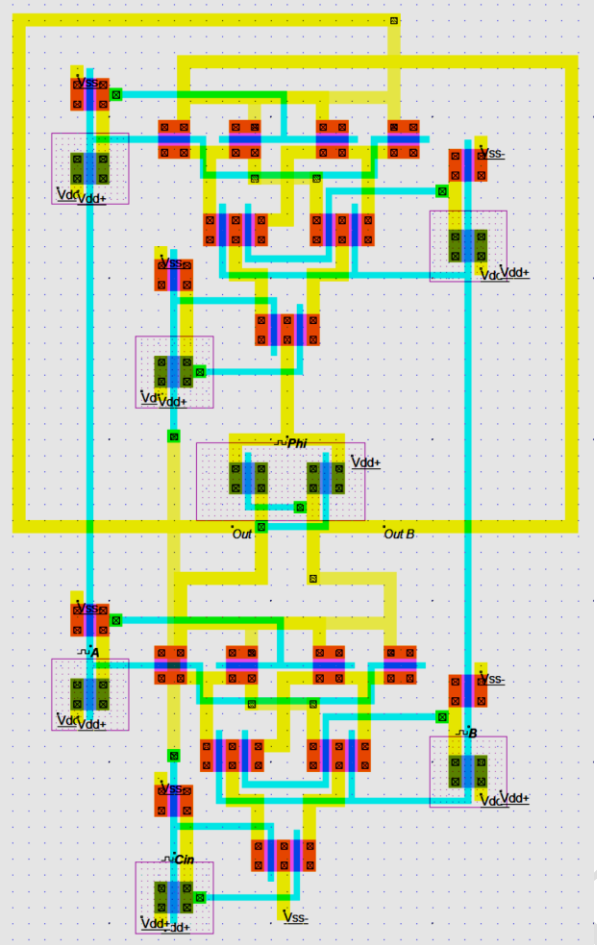

Fig 6. 1-bit Full Adder cell using EEAL

Static traditional CMOS logic style is utilized to actualize the customary Vedic multiplier. If there should arise an occurrence of adiabatic implementation, first we portray the EEAL entryways and after that we show the plan of adiabatic 8x8 Vedic multiplier using EEAL rationale. Complex entryways can be effectively executed by utilizing basic NM OS based DC VS arrange. In Fig. 1, by supplanting the DCVS organize we can implement the AND-NAND entryway with EEAL circuit topology.

DCVS organize for total and convey piece of Full promotion der circuits, alongside AND square is appeared in figure 5. We have planned an adiabatic standard-cell library, comprising of basic computerized doors such as buffer/inverter, two information sources and three-input capacities, snake and multiplier block of differing bit length utilizing Cadence apparition circuit test system in 0.18µ m innovation. W/L proportion of the PMO S and NMOS are brought with W/L = 12λ/2λ and 6λ/2λ where λ=0.9 µm.

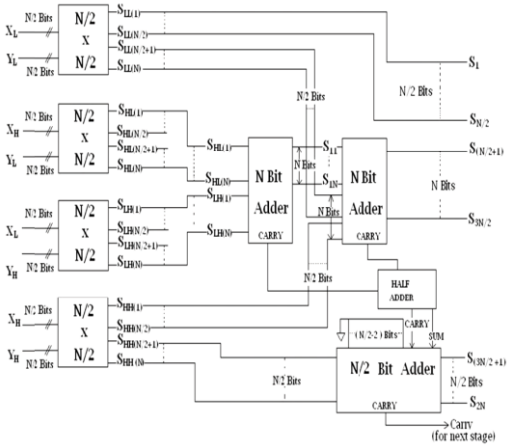

Fig. 7. General block diagram of NxN Vedic Multiplier

IV. PROPOSED ARCHITECTURE

The conventional NxN Vedic multiplier architecture was modified as pipeline Vedic multiplier. In this, pipeline buffers were inserted to increase the throughput of the multiplier. The pipeline vedic multiplier using adiabatic logic family was implemented using 180nm technology. The pipeline Vedic multiplier design is shown below.

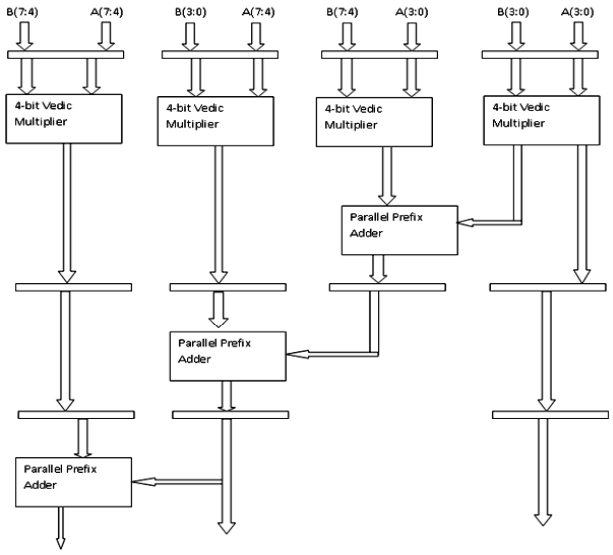

Fig 8. Pipeline Vedic Multiplier

V. CONLCUSION

The EEAL Adiabatic Pipeline Vedic Multiplier was implemented using 0.18 CMOS technology. The proposed pipeline Vedic multiplier using EEAL technique helps to reduce the power consumption enabling for low power operations using adiabatic logic. The results were shown in the below figures.

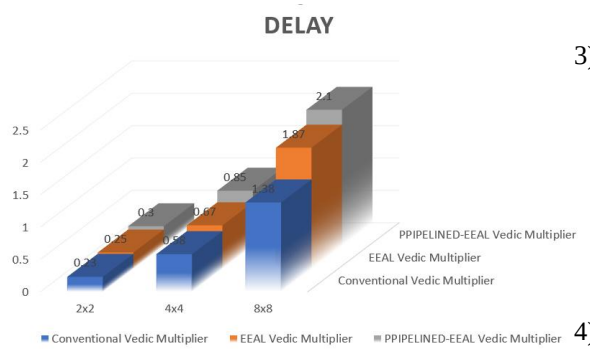

Fig. 9(a) Delay Analysis

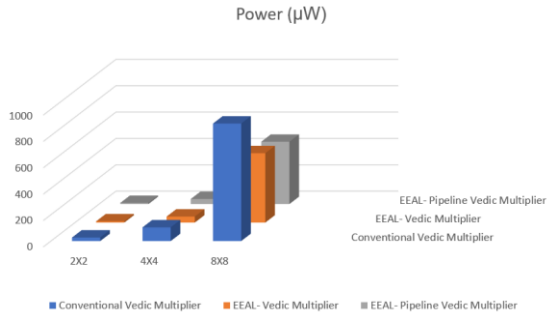

Fig. 9(a) Power Analysis

VI. REFERENCE

1) M. Chanda, S> Banerjee, D. saha and S. Jain, "Novel Transistor Level Realization of Ultra Low Power High-Speed Adiabatic Vedic Multiplier," IEEE Conference, ISBN: 978-1-4673-5090-7 pp. 801–806, April 2013.

2) P. P. Kundu, O. Bandyopadhyay, A. Sinha, "An efficient architecture of RNS based Wallace Tree multiplier for DSP applications," Proceedings 51st Midwest Symposium on Circuits and Systems, Knoxville, TN, pp. 221, 10-13 Aug. 2008.

3) Z. Gang, H. Michalik and L. Hinsenkamp, "Complexity Analysis and Efficient Implementations of Bit Parallel Finite Field Multipliers Based on Karatsuba-Ofman Algorithm on FPGAs" IEEE Trans. on VLSI system, vol. 18, no. 7, pp. 1057-1066.

4) J. Chen, C. H. Chang, "High-Level Synthesis Algorithm for the Design of Reconfigurable Constant Multiplier," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 12, pp. 1844-1856, 2009.

5) M.E Paramasivam and R.S Sabeenian, "An efficient bit reduction binary multiplication algorithm using Vedic methods," IEEE 2nd International Advance Computing Conference, Patiala, India, pp. 25, 19-20 Feb. 2010.